Theory and Measurements of Flip-Chip Interconnects for Frequencies up to 100 GHz

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***Abstract*—A detailed investigation of flip-chip interconnects up to W-band frequencies is presented in this paper. In a coplanar 50-Ω environment, different test structures were fabricated and measured to determine the electromagnetic characteristics of flip-chip multichip modules, such as detuning, reflection at the interconnect, and parasitic coupling. Electromagnetic simulation is used to explain the details behind the measured results. Key to high return loss at the interconnect is a small bump-pad area. Applying simple compensation structures, the frequency range of operation can be further extended. It is shown that a return loss beyond 20 dB in the frequency range up to 80 GHz is achievable along with excellent reproducibility. Measurements on detuning and isolation are also presented.**

***Index Terms*—Finite-difference methods, flip-chip devices, MMIC multichip modules, packaging.**

I. Introduction

THE increasing interest in wireless communications and automotive sensor applications demands for low-cost packaging solutions with excellent millimeter-wave performance. One of the most attractive approaches in this regard are flip-chip based microwave multichip modules (MCMs) [1]–[6]. In order to make full use of the possibilities offered by this technology, a basic understanding of the electromagnetic effects related with the flip-chip scheme with and without housing is indispensable. There are two main issues that determine the millimeter-wave characteristics of a flip-chip-mounted monolithic microwave integrated circuit (MMIC): detuning of the circuit on the chip due to its proximity to the motherboard [7], [8] and the reflection at the bump interconnect [7]–[9]. A package may introduce additional parasitics, primarily with regard to substrate modes, which affect isolation [8], [10].

The purpose of this paper is not only to describe these phenomena, but also to provide design rules, which guarantee optimum exploitation of the millimeter-wave potential offered by the flip-chip technique. Our investigations are based on measurements of flip-chip test structures up to 100 GHz. Three-dimensional frequency-domain finite-difference (FDFD) simulation is applied to obtain insight into the underlying electrical effects. The paper is organized as follows. After a general description of the test structures in Section II, the detuning effect and the reflection at the interconnect are treated in Sections III and IV, respectively. Section V then presents results on package-related parasitics.

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II. Test Structures Fabricated

Previous work, as well as intuitive understanding, suggest that high return loss at the interconnect requires small bump diameters [9]. Therefore, we chose a flip-chip technology for test structure fabrication, which allows miniaturized bump diameters down to 20 μm. Such small bumps can be achieved, for instance, by means of lithographic processes and a deposition by microplating in photoresist cavities combined with Au/Au-thermocompression bonding (TC-bonding) [11], [12]. At the Alcatel Research Center, Stuttgart, Germany, a set of seven test chips was bumped and bonded to a ceramics motherboard. GaAs test chips with different passive coplanar structures were designed and fabricated at the Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany. The bump-pad area on the chips was chosen to be 60 μm $\times$ 60 μm. Bump diameter was varied between 25–35 μm, whereas bump height is kept constant at 22 μm. On-wafer characterization up to 100 GHz was done in-house by means of an HP 8510XF single sweep network analyzer.

In the following, measurements and simulation data concerning the two main millimeter-wave effects of the flip-chip scheme, detuning, and reflection at the bump interconnect are presented.

III. Detuning

Facedown chip mounting is always accompanied by an unwanted detuning effect. The carrier substrate surface comes near to the chip surface, which changes the electrical characteristics of the circuit on the chip. Previous investigations in a 50-Ω coplanar environment have shown that this effect is almost negligible for bump heights h larger than about 0.3 of the ground-to-ground spacing d [7]. Accordingly, for a typical 50-μm-wide coplanar waveguide (CPW), one has a minimum bump height of 15 μm. The situation gets worse when using a metallized motherboard surface below the chip because this arrangement strongly enhances detuning [13] and gives rise to an unwanted parallel-plate mode in the gap between the chip and motherboard [7], [10].

In order to check these findings against measurements, we use a test structure where the change in the effective dielectric constant is translated into the resonance frequency shift of a simple filter structure, which can be detected with much higher accuracy than phase-constant variation of a thru-line. Fig. 1 shows

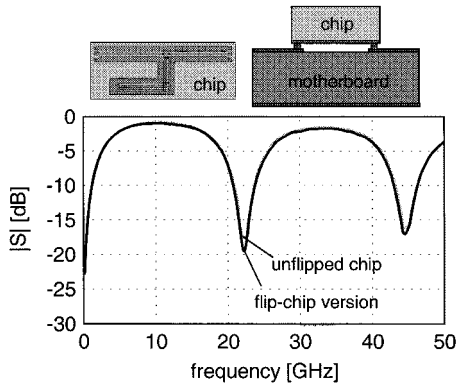

Fig. 1. Insertion loss of a simple filter structure as a function of frequency: comparison of the unflipped and flipped version; the shift in resonance frequency is a measure for detuning (bump height 22 μm and 54 μm ground-to-ground spacing on a GaAs chip).

this structure and its measured insertion loss. The short-circuited shunt stub of a coplanar T-junction acts as a resonator with half-wavelength resonance at 22.5 GHz. Any detuning will affect resonant frequency, which can be determined with high accuracy from the insertion loss curve.

For this purpose, Fig. 1 compares results for the bare chip and corresponding flipped setup. The insertion loss up to 50 GHz is measured with a frequency resolution of 0.5 GHz. As can be seen, the resonance frequencies of the unflipped and flipped chip agree extremely well. Obviously, the frequency shift caused by the flip-chip setup is smaller than the 0.5-GHz frequency resolution used here, which corresponds to a change in characteristic line parameters below 1%. Identical results were obtained for the entire set of seven test structures. This confirms the design rule mentioned above.

IV. Reflections at the Bump Interconnect

A. Main Parameters

According to [7]–[9], the flip-chip interconnect can be described by an effective capacitance. This reactance results from the superposition of a capacitive and an inductive effect. The capacitive part is caused by dielectric loading at the transition due to the presence of both chip and motherboard dielectrics. The inductive contribution stems from the changes in current density distribution and direction when going from the motherboard line via the bump to the chip line. In common structures, the capacitive effect is larger than the inductive. Bump height was found to be of minor importance for reflections and is, therefore, not considered here. The remaining interconnect parameters are as follows:

- bump diameter;
- bump-pad area (length and width);
- dielectric overlap between chip and motherboard;
- total width of the transition (determined by the distance between signal and ground bump).

Their influence is studied in the following by means of FDFD simulation. Fig. 2 displays the flip-chip single transition under investigation and defines the dimensions in the transition area. The CPW-to-CPW case is treated.

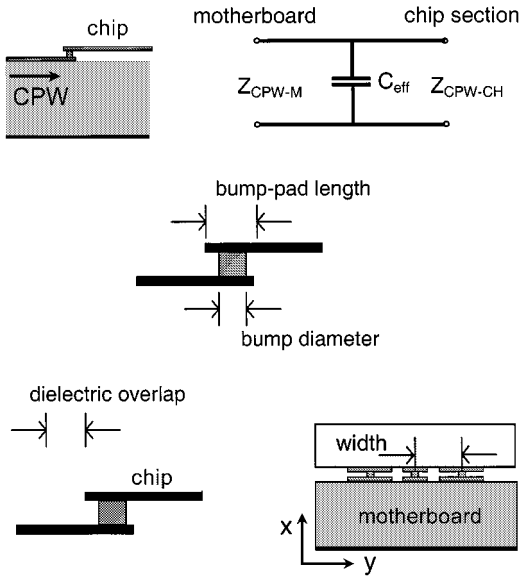

Fig. 2. Flip-chip interconnect, its electrical description, and the dimensions: bump cross section, bump-pad size, dielectric overlap, and, in the cross-sectional view, the width of the transition (center–center).

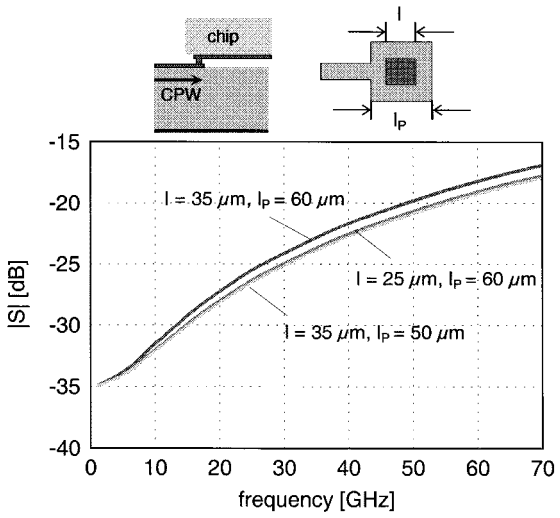

Fig. 3. FDFD simulation data of CPW input reflection against frequency. Parameters are the bump cross section of the interconnect ($l \times l = 25$ and $35\ \mu\text{m}^2$) and the bump-pad length in propagation direction ($l_P = 50, \ldots, 60\ \mu$m); 50-$\Omega$ CPW with 120-μm ground-to-ground spacing on the motherboard and 54 μm on the GaAs chip, respectively.

Fig. 3 presents simulation data of CPW input reflections for the two bump diameters used in the test structures (25 and 35 μm). The results indicate that a 10-μm reduction in bump diameter reduces reflection by less than 1 dB at 70 GHz. The same variation is applied to chip pad-length l_P in propagation direction ($l_P = 50, \ldots, 60\ \mu$m), which results in a somewhat larger decrease. Since, in practice, minimum pad length l_p is determined by the bump diameter, the conclusion is simple: use small-diameter bumps and keep the pad as small as possible.

In Fig. 4(a), the dielectric overlap of chip and motherboard is varied. This parameter is determined by dicing tolerances, etc. Changing the dielectric overlap from a theoretical value of 0–50 μm increases reflection significantly by about 2 dB at 70 GHz. A further extension of the same order, on the other

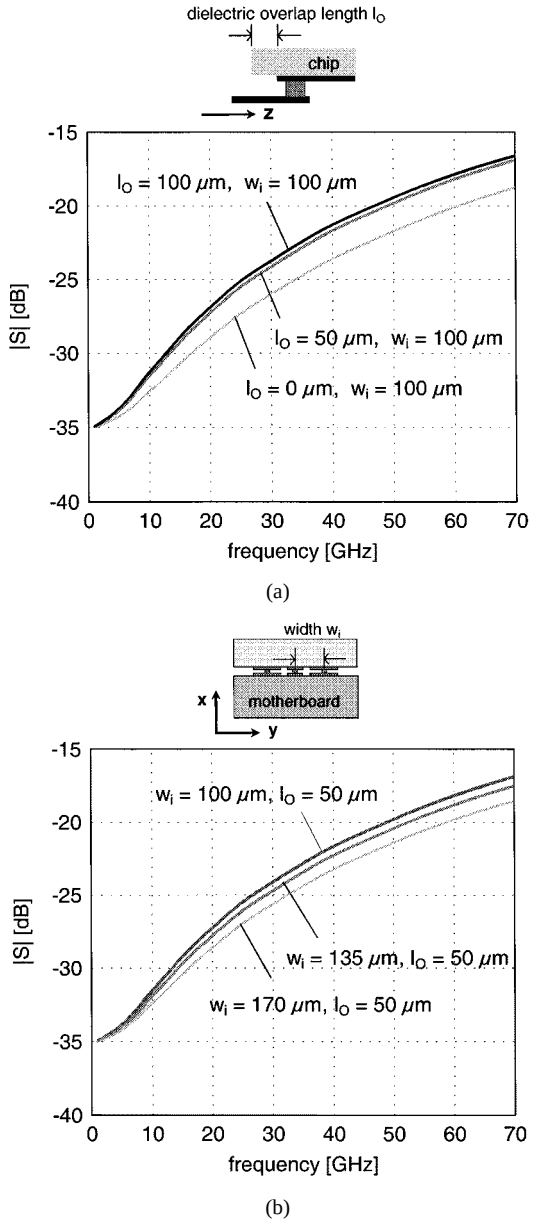

Fig. 4. FDFD simulation data of CPW input reflection against frequency. Parameters are: (a) the dielectric overlap length l_O ($l_O = 0, \ldots, 100$ μm, $w_i = \text{const.}$) and (b) the width w_i of the interconnect ($w_i = 100, \ldots, 170$ μm, $l_O = \text{const.}$). Interconnect data: chip pad-area 60 μm × 60 μm, bump diameter 35 μm, bump height 22 μm, 50-Ω CPW with 120-μm ground-to-ground spacing on motherboard and 54 μm on GaAs chip, respectively.

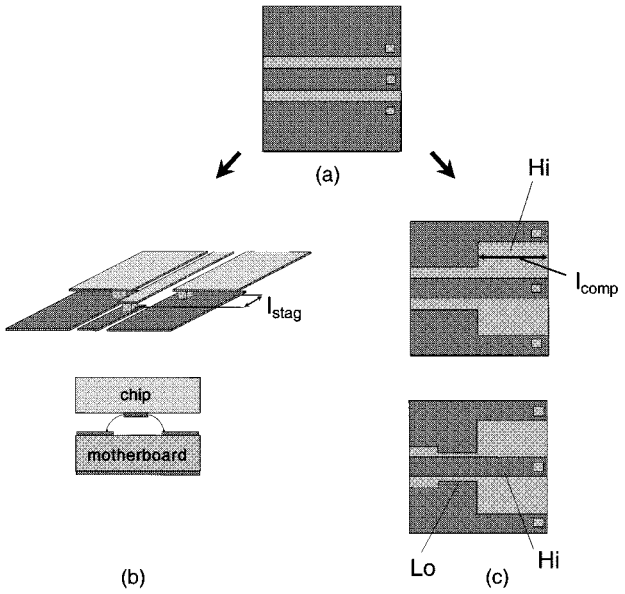

Fig. 5. Optimized interconnect design. (a) Layout on the motherboard without any compensation. (b) Staggered bumps: the forward-pulled center conductor bump leads to a line section with an elevated center conductor. Due to the field concentration in the air region, the characteristic line capacitance decreases. (c) On-motherboard compensation: single high-impedance (Hi) line section at the interconnect and the more complex high–low (Hi–Lo) version. The resonant character of the Hi–Lo structure allows a distinctive reduction of reflection in a selective frequency range (see, e.g., [17]).

hand, does not result in any noticeable change in return loss. This is understandable from physics because only the dielectric next to the interconnect can change capacitance there. In practice, overlap dimensions below 50 μm are unrealistic because if the bump pads are located at the chip edge, dicing tolerances do not allow smaller values. Hence, one should consider this effect during chip layout, but it does not provide room for significant improvements.

The third parameter investigated here is the total width of the transition. For this purpose, the distance between signal and ground bumps is varied from 100 to 170 μm (center–center). Fig. 4(b) shows the results: the larger the distance, the lower the reflection at the interconnect. The improvement amounts to about 2 dB. At a first glance, this is surprising because larger width is expected to increase reflection. More detailed studies reveal, however, that an internal compensation effect occurs at the transition: the longer way of the ground current raises inductance, which compensates capacitance and, consequently, reduces the resulting reflection coefficient. The amount of compensation is limited, however, because the width of the CPW including the ground planes must be smaller than the wavelength in the substrate in order to avoid resonances. Moreover, parasitic coupling into the unwanted substrate mode (parallel-plate line (PPL) mode) increases with metallization width.

In brief, the bump-pad area and, if possible, the dielectric overlap, should be kept as small as possible in order to achieve minimum reflections. Due to an internal compensation effect, the return loss can be further improved to a certain extent by choosing a larger distance between signal and ground bumps.

B. Optimized Design

Thus, the first thing to do is to shrink the bump-pad area. This, however, is limited by the bump diameter, which is related to the flip-chip technology applied. Bump diameters in the range of 50 μm and below are possible [11], [12], but not readily available from the common processes. Therefore, it is important to know what one can do from a circuit designer's point-of-view to optimize millimeter-wave properties of the interconnect. This will be discussed in the following. The basic idea is that of compensation, i.e., reducing the excess capacitance at the transition by adding an inductive counterpart. Two approaches are investigated here: firstly, staggered bumps [14], [15] and, secondly, an on-motherboard solution employing a high-impedance line section [16]. Fig. 5 illustrates these two solutions.

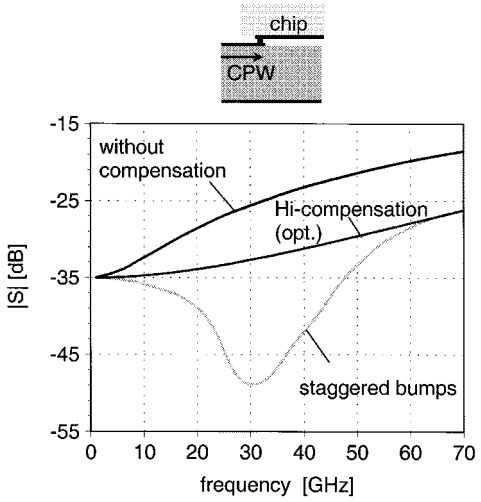

Fig. 6. Optimized design of a flip-chip interconnect by means of compensation: CPW reflection as a function of frequency (3-D FDFD simulation data) comparing the following three different cases: 1) uncompensated; 2) staggered bumps designed broad-band below 50 GHz; and 3) on-motherboard Hi compensation designed for optimum behavior at 70 GHz. The dimensions are: staggering length $l_{\rm stag} = 144.5$ μm, bump-pad area 60 μm $\times$ 60 μm, bump cross section 35 μm $\times$ 35 μm, bump height 22 μm, dielectric overlap 0 μm, distance w_i between signal bump, and center conductor bump 100 μm (center–center).

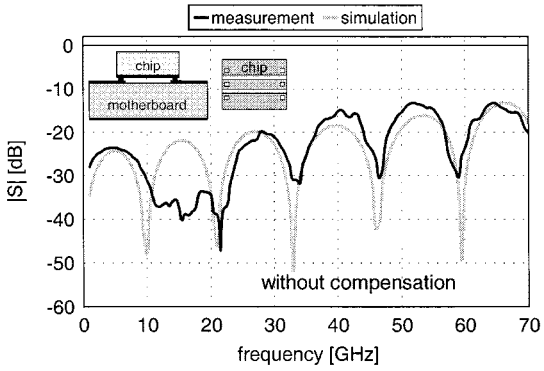

Fig. 7. Measured and simulated reflection against frequency for a back-to-back test structure without compensation. Interconnect data: chip pad area 60 μm $\times$ 60 μm, bump diameter 35 μm, bump height 22 μm, dielectric overlap 50 μm, distance w_i between signal bump and center conductor bump 100 μm (center–center), 50-Ω CPWs with 120-μm ground-to-ground spacing on the motherboard and 54 μm on the GaAs chip, respectively.

In the first example, compensation is achieved by staggering center conductor and ground bumps. Fig. 5(b) demonstrates the main effect: the center conductor of the chip is elevated and the field concentrated in the air region, which leads to a decrease in capacitance. Alternatively, with the on-motherboard approach, a suitable impedance transformation network is realized on the motherboard next to the interconnect. The most simple version is a short line section of high characteristic impedance [see Fig. 5(c)], but also more complex topologies may be employed, e.g., a two-stage compensation consisting of a Hi–Lo structure, also illustrated in Fig. 5(c).

In order to check effectiveness of the compensation techniques, a flip-chip transition according to Fig. 3 is analyzed by means of FDFD simulation. A bump cross section of 35 $\times$ 35 μm^2 and a 60 $\times$ 60 μm^2 bump pad are chosen. The resulting reflection of the CPW mode is plotted in Fig. 6. The staggered approach requires a compensation length $l_{\rm stag}$ of 145 μm. This value was obtained by an optimization carried out broad-band in the frequency range below 50 GHz. A significant reduction in reflection coefficient is observed up to 70 GHz. At about 30 GHz, the capacitive behavior changes to an inductive one, which leads to a minimum in magnitude and results in a distinctive increase in reflection up to -26 dB at 70 GHz. The clear disadvantage, however, is that the interconnect now consumes additional expensive chip area. Moreover, this approach is not compatible with common chip layouts, but requires a customized chip design. The optimum staggering length can be determined only by a computationally expensive three-dimensional (3-D) electromagnetic simulation. In brief, this approach is effective, but not generally recommendable.

The on-motherboard approach, on the other hand, affects the motherboard side only. Using the most simple transformation, a single high-impedance line section, about 7-dB improvement in return loss, can be achieved (see Fig. 6). This result can be further enhanced employing a two-stage compensation realized by a Hi–Lo structure, as shown in Fig. 5(c). Such a Hi–Lo compensation was successfully applied in [17] for a structure with larger bumps, which documents feasibility of the approach. Although this Hi–Lo compensation is narrow-band on principle, the usable bandwidth still spans several tens of gigahertz, which is considerably more than for comparable compensated bond-wire interconnects. Further extensions of this approach would lead to a filter design with well-placed resonances. In brief, compensation by CPW circuit elements on the motherboard side is a cost-effective and simple approach. Moreover, once a model of the transition is available, this compensation can be designed by commercial circuit design software and does not necessarily require 3-D electromagnetic tools.

C. Verification by Measurements

In order to validate the simulation results, the flip-chip test structures described in Section II were characterized. They include compensated transitions, both staggered bumps and a high-impedance compensation on motherboard. First, a brief verification of our simulation results is given by Fig. 7. It presents measured and simulated reflections of a flip-chip back-to-back structure with a coplanar thru-line on chip and without any compensation in the interconnect area. The agreement is excellent, which validates the model and proves accuracy of our finite-difference frequency-domain code (the differences around 15 GHz are attributed to a resonance effect with the neighboring line structures on the chip, which are not accounted for in the simulation).

In a second step, measurements of the uncompensated structure are compared with both versions of compensation. More precisely, three different interconnects are considered here: firstly, the uncompensated case as above as a reference, secondly, staggered bumps, and, thirdly, a transition with an on-motherboard high-impedance section, optimized for 70 GHz. On-wafer measurements up to 100 GHz are presented in Fig. 8.

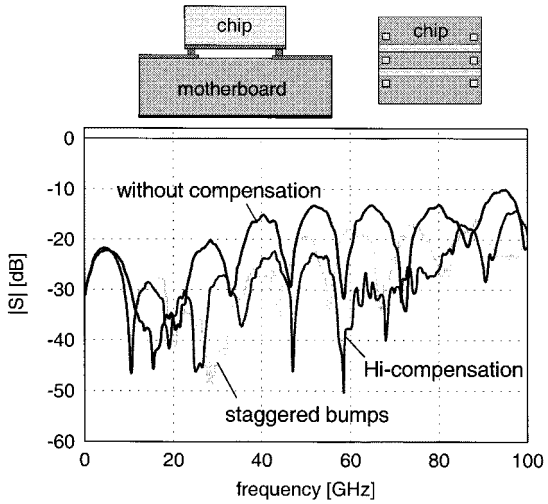

Fig. 8. Reflections of the test structures without and with compensation as a function of frequency (CPW and interconnect data as in Fig. 7). The high impedance compensation (Hi-compensation) is designed for optimum behavior at 70 GHz, whereas the staggering length is chosen for a broad-band design below 50 GHz.

The measurement data show excellent performance up to millimeter-wave frequencies. The return loss of the uncompensated case stays below the −20-dB level up to 37 GHz, which demonstrates the potential of the technique used. Moreover, the effectiveness of the compensation approach is verified clearly. Staggered bumps offer a return loss beyond 20 dB up to 58 GHz. The minimum in reflection around 30 GHz is in agreement with the behavior of the single transition shown in Fig. 6. Looking at the results for the high-impedance compensation, a further significant improvement is observed: reflections remain below −20 dB up to 82 GHz. Note that this data refer to the back-to-back structure that includes two flip-chip interconnects. Thus, reflections at a single interconnect are 6 dB below the maximum shown here. Insertion loss per transition is smaller than 0.2 dB up to 90 GHz and, thus, in the order of measurement accuracy (0.3 dB for the uncompensated case).

Comparing the return-loss level of the staggering and Hi approaches, one should mention that both compensation concepts can provide similar results, depending on the structure designed. If the simple Hi variant does not reduce the reflection sufficiently, the Hi–Lo compensation can be chosen, which allows further improvement. The disadvantage of the staggering approach is not its electrical behavior, but the area consumption on chip.

Besides the return-loss data, reproducibility is a key issue regarding system application. In order to clarify this, Fig. 9 presents measurements data of the Hi compensation for the whole set of seven test structures. The deviations are almost negligible. Reflections remain below −20 dB up to 82 GHz for all seven samples. This impressive result reveals that this is not a single best value, but can be maintained also in a larger MCM lot. Moreover, since the samples have two different bump diameters of 25 and 35 μm, these measurements verify the above-mentioned results, stating a minor influence of bump diameter variation (see Section IV-A).

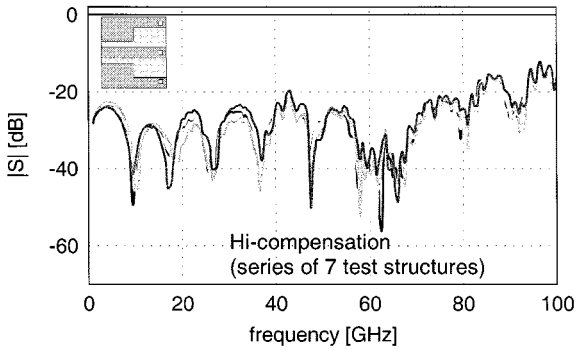

Fig. 9. Reflection against frequency for a series of seven test structures (for CPW and interconnect data, see Fig. 7, the series contains sample with two different bump diameters of 25 and 35 μm).

One concludes that flip-chip interconnects allow extremely low reflective interconnects because of their small dimensions and are, therefore, suitable for millimeter-wave applications up to the W-band. Even with larger bump geometries, as obtained by a common solder process or stud bumps, for instance, the flip-chip technique offers good millimeter-wave properties if compensation measures are applied.

V. Package-Related Parasitics

Inserting a flip-chip structure into a housing, one has to take into account package-related parasitics. In a coplanar environment, special attention has to be paid to substrate moding [8], [10]. Usually, a conducting backside is present, formed by the bottom of the package or the chuck during on-wafer measurements. As a consequence, an unwanted mode, i.e., the parasitic PPL mode, has to be considered, which represents the floating potential between CPW ground planes on top of the motherboard and the backside. Below the chip, this mode has a different characteristic because it extends from the backside metal of the motherboard to the CPW metal on the flipped chip and, thus, includes the air gap between the motherboard and chip [see Fig. 10(a)]. Hence, its effective permittivity is smaller than that of the conventional PPL mode.

In order to avoid package-related malfunctions in flip-chip-based coplanar millimeter-wave MCMs, parasitic coupling phenomena due to the unwanted substrate mode must be accounted for. Until now, a simple way to suppress this additional mode is not known. Therefore, the crosstalk issue is of high priority regarding system applications. Recent simulation work [8] reveals strong resonance peaks caused by the PPL mode and demands for a more comprehensive investigation.

The test structure shown in Fig. 10(a) is used to demonstrate and quantify parasitic crosstalk (a similar setup was applied in [10]). A passive GaAs chip with two opposite CPW short stubs is flip-chip-bonded to a ceramics motherboard. Due to the large distance in the order of 2 mm between the stubs, CPW coupling between the stub vanishes. Due to the conducting backside, however, the PPL mode will propagate between both ports and cause nonzero transmission.

Fig. 10(b) presents the measured transmission coefficient of the bare chip before mounting and after flip-chip bonding. In

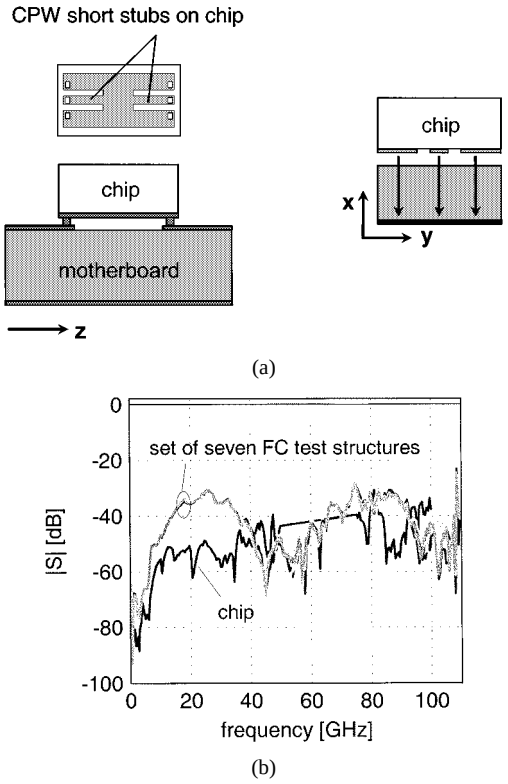

Fig. 10. Test structure for crosstalk measurements. (a) Chip layout with two opposite CPW short stubs (stub lengths 1100 and 1300 μm, respectively, the distance between is about 2 mm, interconnect data as in Fig. 7) and field pattern of the PPL mode in the chip area. (b) Transmission coefficient of the flip-chip version against frequency (0.15, . . ., 110 GHz) in comparison with data for the bare chip before mounting (0.15, . . ., 50 GHz and 75, . . ., 110 GHz).

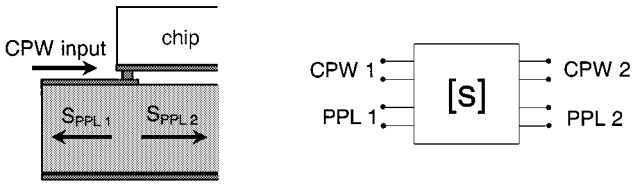

Fig. 11. Flip-chip single transition and the appropriate electrical four-port. A part of the incoming CPW signal is scattered at the bump-pad discontinuity into a forward (S_{PPL2}) and backward (S_{PPL1}) PPL mode.

the unflipped case, parasitic coupling on the chip is in the order from -50 to -40 dB. After flip-chip bonding, its value increases to about -30 dB. The curve measured on-wafer does not exhibit package-induced resonance peaks, but a smooth half-wavelength resonance of the short stubs with a minimum around 50 GHz.

In order to obtain a better insight into the coupling effects, the structure in Fig. 10(a) was analyzed in more detail using the FDFD method. The frequency-domain treatment allows mode separation and, thus, offers the possibility of different port terminations for the CPW and the PPL mode. Fig. 11 illustrates the electrical four-port used to describe the setup.

- A single flip-chip transition can be represented as a four-port with scattering matrix (S). The incoming CPW signal at port (1) is scattered at the bump interconnect not only in CPW modes, but also into a forward and backward PPL mode. Simulations show that coupling into the PPL mode in the forward direction (S_{PPL2}) is in the order of -20 dB, a value comparable to the CPW reflection. In contrast, transmission into the backward PPL mode (S_{PPL1}) remains smaller, with magnitude values in the order of -30 dB.
- The PPL mode is almost unaffected by the CPW structure on top of the motherboard as far as the ground metallization there is not interrupted. More difficult is the situation at the outer PPL ports, which refer to the boundaries of the motherboard. There, a reflection coefficient r_{PPL} is assumed. In the usual packaged case, the sidewalls of the housing connect the CPW ground planes with the backside, thus forming a short circuit for the PPL mode (i.e., $r_{\mathrm{PPL}} = -1$). During on-wafer measurements, the edge of the motherboard is free and instead represents an open-boundary condition for the PPL mode. To this open circuit, however, we have a parallel path, the unknown impedance of the probes seen by the PPL mode. This point can be clarified comparing measurements with simulation data.

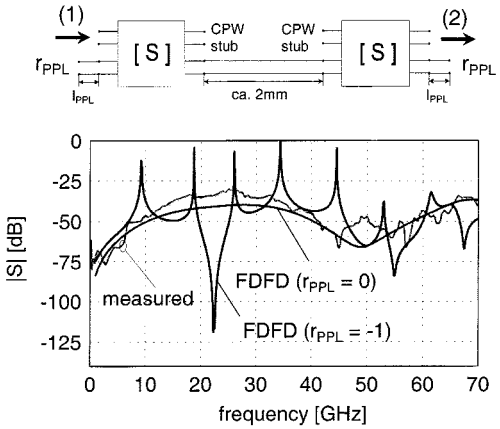

Fig. 12. Measured and simulated transmission between CPW stubs of the flip-chip setup in Fig. 10. Simulation data is based on the two-mode representation shown above with scattering matrix (S) calculated by the FDFD method. The reflection coefficient r_{PPL} at the outer PPL ports is varied as specified ($r_{\mathrm{PPL}} = 0$ and -1).

In Fig. 12, the measured transmission between the stubs [see Fig. 10(a)] is compared to simulation results according to the model given in the upper part of the figure. Two different values for the reflection of the PPL mode r_{PPL} at the outer ports are assumed, i.e., $r_{\mathrm{PPL}} = 0$ (the matched case) and $r_{\mathrm{PPL}} = -1$ (the ideal short), which corresponds to the short-circuit condition. One finds close agreement between measurements and simulation for $r_{\mathrm{PPL}} = 0$, which means: a matched condition for the PPL mode is effective. This leads to the conclusion, that the probes act as an absorber for the PPL mode, representing a parallel path to the boundary effect of the substrate.

Note, however, that this statement applies to the on-wafer measurement setup only. In a package, one has a different situation since usually the CPW ground planes are connected to the conducting backside of the substrate, formed by the bottom of the housing, at least at a coaxial-type feedthrough. This configuration represents approximately a short circuit for the PPL mode. Thus, the package walls (and any vias) form a low-loss half-wavelength resonator for the PPL mode, which is coupled

to the CPW transmission lines at each bump interconnect. This leads to peaks in the transmission coefficient under a resonance condition, as observed in Fig. 12 for the case $r_{\mathrm{PPL}} = -1$, which may cause severe circuit instabilities, although coupling to the PPL mode at each flip-chip interconnect is only in the $-$20-dB range. This means: even if isolation is acceptable under on-wafer measurement conditions, one might experience difficulties when putting the structure in a metallic housing with coaxial feedthroughs. Low parasitic coupling under measurement conditions does not guarantee stability under real circuit applications. Of course, these effects are of particular importance for systems where high gain or high input–output isolation is required [4].

The more general consequence is that it does not suffice to consider a flip-chip interconnect isolated from the way the structure (primarily the motherboard) is packaged. Beside chip detuning effects and the return loss of the bump interconnect, one has to include coupling to the PPL mode and suitable measures to suppress it. In other words, developing an optimized flip-chip approach must include the individual packaging solution of the motherboard.

VI. Conclusions

- Flip-chip interconnects provide excellent performance up to 100 GHz. In order to obtain low reflections at the interconnect, the higher the operating frequency, the smaller the transition area should be designed. First-order parameters in the millimeter-wave frequency range are the bump diameter and, related to this, the bump-pad area.
- Bump height h only affects chip detuning. It should be larger than 15 μm for a CPW with 50-μm ground-to-ground spacing d, or, more general, the ratio h/d should be larger than about 0.3 for coplanar chips. Measurements of an on-chip filter resonance support this finding.
- Minimized bump-pad sizes down to 60 μm $\times$ 60 μm and bump heights in the order of 25 μm are achievable, for instance, with Au-electroplated bumps bonded by thermocompression. For such dimensions, a reflection below $-$20 dB up to 40 GHz is feasible without any further optimizing.
- For a given bump-pad geometry, return loss can be further improved by compensation. As demonstrated by measurements on test structures, a simple modification of the line section at the interconnect already yields reflections below $-$20 dB up to 82 GHz. The insertion loss per transition is below 0.2 dB in this frequency range.
- As could be assessed from a series of seven chips, reproducibility of measured results is excellent. A variation of the bump diameter between 25 and 35 μm was found to be negligible.
- If a conducting backside of the motherboard is present, this introduces substrate moding and causes parasitic coupling. Isolation values of about 30 dB are measured and simulated, which, may lead to unwanted resonance peaks of much higher amplitude in a packaged situation. This means that packaging of the entire MCM is an issue that has to be included in optimization of the flip-chip interconnect from the beginning. New motherboard solutions such as thin-film structures, multilayers, etc. have to be investigated to develop cost-effective packaging techniques with acceptable millimeter-wave properties.

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